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1. OUTLINE OF FUNCTIONS AND FEATURES

1.1 Outline of Functions

The YM2151 is an FM-type sound generator equipped with an 8 bit bus line and capable of producing superb audio quality via a microprocessor program. When this IC is used in tandem with the specially-developed YM3012 D/A converter, you can obtain 8-note, left-right/2-channel audio signals.

In addition, this unit is equipped with noise, vibrato, an amplitude modulation circuit, a sound effects circuit, and timer.

The package is a 24-pin dual in-line package.

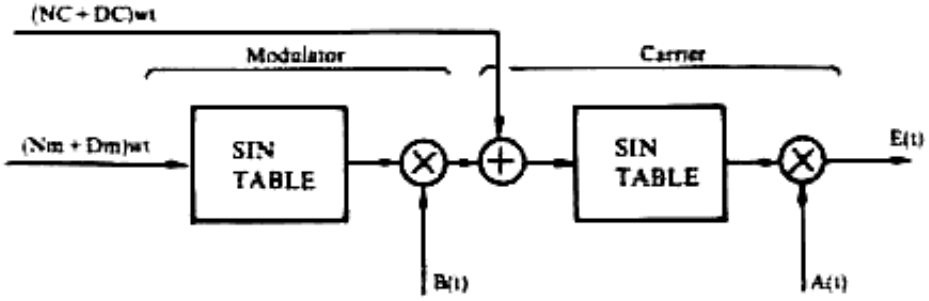
1.2 Features

- Generate up to 8 notes.
- Generate noise.
- Timbre can be altered temporally.
- High harmonic can be de-harmonized from the base frequency.
- De-harmonize between octaves.
- Interval settings of up to 1.6 cents.
- Add vibrato and amplitude modulation.
- Generate a variety of sound effects by extreme de- harmonization of the high harmonic from the base frequency and massive vibrato and amplitude modulation.

1.3 Summary of the Principles of FM-type Sound Generation

FM-type sound can be expressed via a basic configuration like that depicted in Figure 1.1. If this were to be expressed formally, it would look like this:

Fig. 1.1



$E(t) = A(t) \cdot \sin[(Nc + Dc) \cdot wt + B(t) \cdot \sin(Nm + Dm) \cdot wt]$

A(t) : Volume envelope
B(t) : Timbre envelope
Nx : 1/2 of the basic pitch or multiple value
Dx : 1/2 of the basic pitch (1.6 cents) harmonic value

For example, when B(t) = 0, you get a sine wave of (Nc + Dc) times with respect to the basic pitch. In this case, if we assume values for Nc and Dc like those given above, we will obtain a 1/2 the basic pitch or a sine wave of multiple value. As long as the value for Dc is not 0, the output will indicate a pitch sine wave slightly offset from 1/2 the basic pitch or multiple value. When B(t) is greater than 0, the output will not be a sine wave but a wave form including a high harmonic component, because B(t) • sin (Nm + Dm) • wt is added onto the (Nc + Dc) • wt phase information. It therefore follows that a variety of wave forms including a high harmonic component can be obtained by selecting different values for B(t) and (Nm + Dm). Also, the timbre can be altered and output by temporal adjustment of B(t).

Actual output patterns when altering the value of B(t) and (Nm + Dm) and adding it onto the previous pattern are indicated in Fig. 1.2 ~ 1.9.

Fig. 1.2
(Nc + Dc)/(Nm + Dm) = 1, B(t) = 0

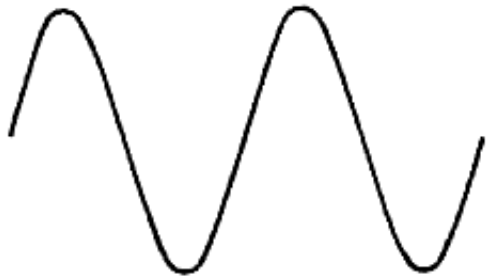


Fig. 1.3
(Nc + Dc)/(Nm + Dm) = 1, B(t) = 0.5

Fig. 1.4
(Nc + Dc)/(Nm + Dm) = 1, B(t) = 1.0

Fig. 1.5
(Nc + Dc)/(Nm + Dm) = 1, B(t) = 1.5

Fig. 1.6
(Nc + Dc)/(Nm + Dm) = 1, B(t) = 2.0

Fig. 1.7
(Nc + Dc)/(Nm + Dm) = 0.5, B(t) = 0.5

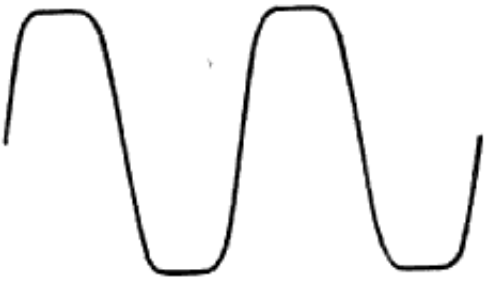
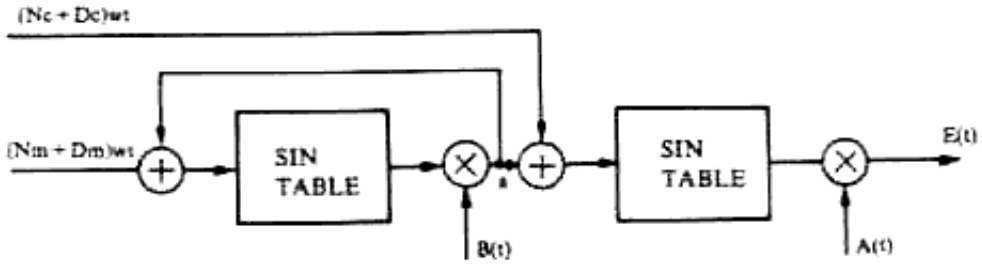


Fig. 1.8
(Nc + Dc)/(Nm + Dm) = 0.5, B(t) = 1.0

Fig. 1.9
(Nc + Dc)/(Nm + Dm) = 0.5, B(t) = 1.5

The YM2151 is equipped to handle 7 different kinds of combinatory connection methods, with two circuits composed of this basic structure assigned to a single note, which can be arranged serially or in parallel, or made to act as only a sine- wave sound source. In addition, with the unit set up as in Figure 1.10, with inclusion of a circuit that takes one's own output signal and returns it to oneself, virtually any type of wave form can be obtained via proper adjustment.

Fig. 1.10



An example of the wave form in this case is depicted in Figure 1.11

Fig. 1.11
Example output of a-point waveform.

2. CONSTRUCTION AND FEATURES

2.1 Block Diagram

The block diagram is as depicted in Figure 2.1.

As explained in the previous section, the YM2151 uses two FM modulation circuits for a single note. These are time division circuits, with sine table read four times. Since it is possible to produce up to 8 sound sources overall, the circuit has been constructed so as to operate on a 32-slot time division basis. Figure 2.2 shows the relation between the sound channel number and the slot number. The following is an explanation of the functions of each of the components, along with the content of the data these components handle.

2.1.1 REG: Register

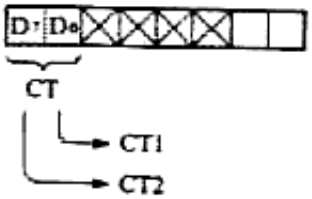
This is 256-byte area register for the storage of data which in turn drive and set the individual function circuits to be explained later. The address map is shown in Figure 2.3. When this register is at initial clear ($\overline{IC}$ terminal = "0"), all is "0" level.

- B: WRITE BUSY FLAG (READ MODE)

  The bit in the diagram below is shown being written in. From the time the write command is received until the write is completed, a period of ΦM 68 bits is required. During this time the flag reads "1". When continuing data and writing in, it is necessary to confirm that this flag reads "0" before writing in the next datum.

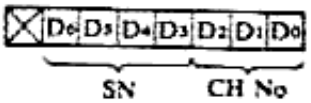
- CT: CONTROL OUTPUT

  Bits D_6 and D_7 correspond to output terminals CT1 and CT2 and comprise the External control output port. At initial clear ($\overline{IC}$ terminal = "0"), the CT_1 and CT_2 terminals read "0" level.



- KON: KEY ON

  As shown in the figure below, when entering a key on (off) which corresponds to a 3-bit channel number and a 4-bit slot, the sound source begins (ends). Writing in "1" for the level at SN turns the key on, while writing in "0" turns the key off. For the channel number please refer to the channel number in Figure 2.2. The SN bits D_3, D_4, D_5, and D_6 correspond to M_1, C_1, M_2 and C_2.

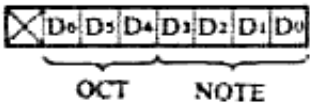


2.1.2 PG: Phase Generator

The phase information needed to fix the carrier frequency and modulator frequency is generated here by KC, KF, MUL, DT1, DT2, PMS data from the REG. Also, the production of vibrato effects by data from the LFO and sound effects due to frequency modulation, etc. is carried out at the PG.

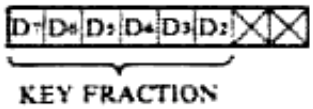
- KC: KEY CODE (OCT, NOTE)

  The key code uses a datum per note, and a datum is composed of 7 bits as depicted in the figure below. The first 3 bits express the octave (8 octaves), and the last 4 bits express the note. The relation between octaves and notes on the one hand and intervals on the other is depicted in Figure 2.4. A sound frequency of 440.0 Hz can be obtained by setting the device clock frequency at 3.579545 MHz and entering frequency data KC:(OCT = 4, NOTE = 10), KF = 0, MUL = 1, DT1 = 0, DT2 = 0, PMS = 0.



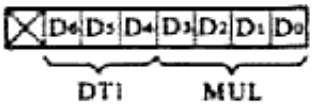
- KF: KEY FRACTION

  The key fraction uses a datum per note, and a datum is composed of 6 bits as depicted in the figure below. With these 6 bits of data you can fix the phase information by dividing the note interval (100 cents) into 1.6-cent segments (see Figure 2.4).



- MUL: PHASE MULTIPLY

  Four data set one note, comprised of 4 bits as indicated in the figure below. With this function you can multiply the KC- and KF-input phase information, as shown in Figure 2.5.

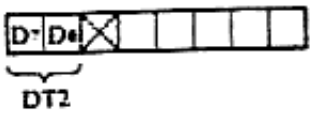


- DT1: DETUNE (1)

  Four data set one note, comprised of 3 bits as indicated in the figure above. With this function you can detune the phase information from the frequency vis-a-vis the KC- and KF-input phase information, as shown in Figure 2.6. Also, the phase information from this DT1 undergoes scaling via the key code.

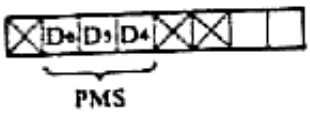
- DT2: DETUNE (2)

  Four data set one note, comprised of 2 bits as indicated in the figure below. With this function you can carry out gross detuning of the phase information from the frequency vis-a-vis the KC- and KF-input phase information, as shown in Figure 2.7. This is effective when generating sound effects.



- PMS: PHASE MODULATION SENSITIVITY

  One datum used to set a note, comprised of 3 bits as indicated in the figure below. You can obtain vibrato and trembling sounds from the LFO (low frequency oscillator) signals that express band width in 8 bits by adding them to the KC and KF. As indicated in Figure 2.8, this sensitivity can be controlled at 8 different levels. The value indicated here obtains when the LFO output is at its maximum value.

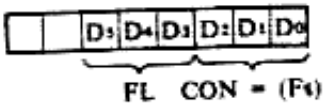


2.1.3 OP: FM Operator

Picks up the phase information from the PG and reads out the sine table. The read-out signal is multiplied by the envelope information from the EG. At end of OP circuit, connection switch is activated, or you can control the volume of feedback the phase information as necessary. Here, the FM-modulated signal is transmitted to ACC.

- CON: CONNECTION

  One datum used to set a note, comprised of 3 bits as indicated in the figure below. With this CON, you can construct a distinct 8-note OP circuit configuration that will allow you to produce all 8 notes with various timbre.
  Figure 2.9 shows this circuit construction.

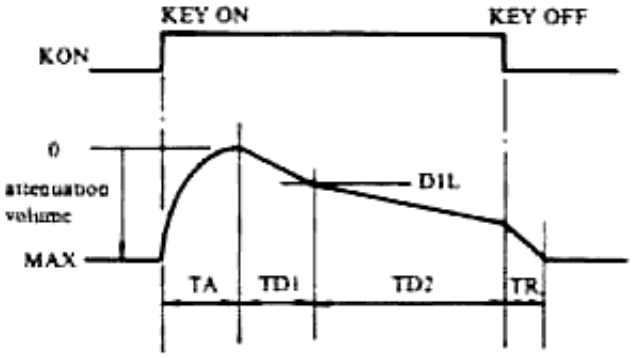


- FL: SELF FEEDBACK LEVEL

  One datum used to set a note, comprised of 3 bits as indicated in the figure above. The FL level can be controlled for all notes as shown in Figure 2.10.

2.1.4 EG: Envelope Generator

The EG output is multiplied by the signal appearing after the OP reads out the sine table, imparting timbre and volume alterations. When the key on is entered at the EG, the EG changes in the manner indicated in the following figure.

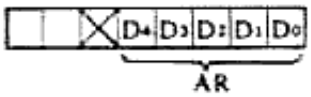


When the attenuation volume is expressed as a logarithm, the attack changes exponentially and the decay changes in a straight line.

The movement from TA to TD1, as well as from TD1 to TD2, is carried out when the attenuation volume is 0 dB, as well as at the first decay level (D1L).

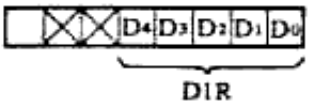
- AR: ATTACK RATE

Four data used to set a note, comprised of 5 bits as indicated in the figure below. When key on is entered at the EG, the attenuation volume diminishes, and after the attack time (TA) the attenuation volume approaches 0 dB. The attack time can be set by means of the AR as in Figure 2.11. Also, the AR is scaled by the key code, so refer to Figure 2.12.



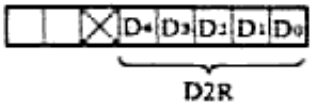
- D1R: FIRST DECAY RATE

Four data used to set a note, comprised of 5 bits as indicated in the figure below. When the attenuation volume is 0 dB, the EG automatically moves to first decay, obtaining first decay level. This first decay time (TD1) can be set by means of the D1R as in Figure 2.11. Also, D1R is scaled by the key code, so refer t Figure 2.12.



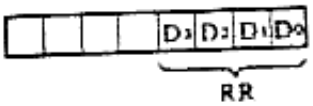
- D2R: SECOND DECAY RATE

Four data used to set a note, with a datum comprised of 5 bits as indicated in the figure below. When the first decay level has been passed, the EG automatically moves to second decay and remains in this state until key off. This second decay time (TD2) can be set by means of the D2R as in Figure 2.11. Also, D2R is scaled by the key code, so refer to Figure 2.12.



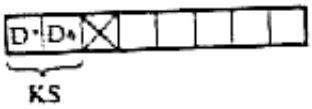
- RR: RELEASE RATE

Four data used to set a note, with a datum comprised of 4 bits as indicated in the figure below. With key off the EG begins release and attenuation advances toward the maximum attenuation volume (96 dB). The release time (TR) can be set by means of the TR as in Figure 2.11. Also, RR is scaled by the key code, s refer to Figure 2.12. Note that because the RR contains one less bit than either D1R or D2R, resolution will be poor.



- KS: KEY SCALING

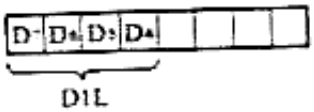
Four data used to set a note, with a datum comprised of 2 bits as indicated in the figure below. The KS scales the AR, D1R, D2R, and RR rates according to the key code, and this scaling can be controlled via four different levels as indicated in Figure 2.12.



The attack, first decay, second decay, and release times are set by each rate after it has been scaled.

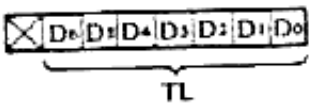
- D1L: FIRST DECAY LEVEL

Four data used to set a note, with a datum comprised of 4 bits as indicated in the figure below. When EG passes this level it automatically moves from first decay to second decay. With a 3 dB resolution, each bit weighted as indicated in Figure 2.13.



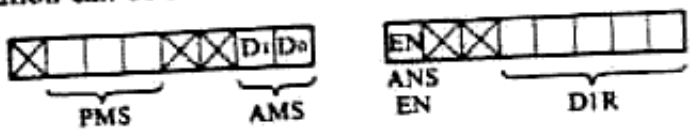
- TL: TOTAL LEVEL

Four data used to set a note, with a datum comprised of 7 bits as indicated in the figure below. The EG calculates the total level (expressed as attenuation volume) operated by the EG with respect to each time and outputs this figure to the OP, controlling the timbre (modulation) as well as the volume. Minimum resolution is 0.75 dB, with the bits weighted as indicated in Figure 2.14.



- AMS: AMPLITUDE MODULATION SENSITIVITY

One datum used to set a note, comprised of 2 bits as indicated in the figure below. The EG can carry out amplitude modulation using (8-bit) LFA data from the LFO. Maximum amplitude modulation can be set as indicated in Figure 2.15.



You can decide whether or not to modulate a particular slot by using the AMS-EN switch when carring out amplitude modulation. AMS data is set for every channel.

2.1.5 NOISE: Noise Generator

When the NOISE control is on ENABLE, the 32nd slot is changed to the noise slot. The noise OS is controled by the NOISE GENERATOR clock externally and can be changed. Also, the envelope uses the 32nd slot for the envelope function, but at this point transformations are not logarithmic: the attack undergoes exponential change and the decay undergoes straight-line change.

- NE: NOISE ENABLE

NE is available if the (D_7) bit is set at "1", making the 32nd bit slot the noise slot.

- NFRQ: NOISE FREQUENCY

The relation between NFRQ and noise frequency is

$$f_{NOISE}(KHz) = \frac{\phi_M\ (KHz)}{32*(NFRQ.)} \qquad \phi_M = 3579.545KHz \quad \text{(YM2151 added clock frequency)}$$

and can be changed throughout a range of from approximately 3.5 kHz to 111.9 kHz.

At this point the noise period value is

$$T_{NOISE}(SEC) = \frac{2^{17}-1}{f_{NOISE}(Hz)}$$

and can range from approximately 37.5 sec to 1.17 sec.

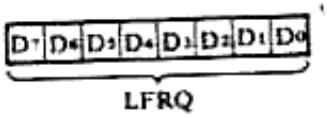
2.1.6 LFO: Low Frequency OSC

The LFO, which can control oscillation waves over a wide spectrum (from approximately 53 MHz to 0.008 Hz), selects one wave form from among several available, providing sound source frequency modulation and amplitude modulation.

At this point, the output level can be controlled with the signals used for the frequency modulation and amplitude modulation.

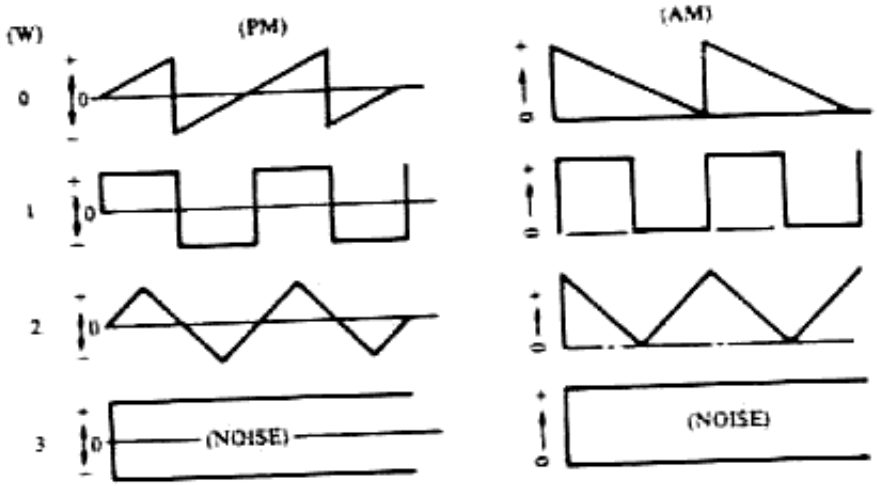
- LFRQ: LOW FREQUENCY

  With the following 8 bits the oscillation frequency can be set as indicated in Figure 2.16.



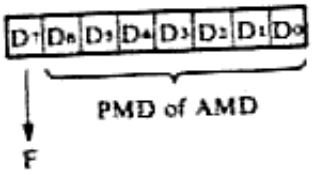
- W: WAVE FORM

  With the following 2 bits 4 different types of frequency (PM) and amplitude (AM) modulation can be output.



- PMD/AMD: PHASE MODULATION DEPTH/AMPLITUDE MODULATION DEPTH

  Each datum is composed of 7 bits, with the data assigned to the first bit distinguishing between PMD and AMD. The PMD and AMD control the frequency modulation/amplitude modulation signal output level to a resolution of 1/128. As you may have guessed from the previous section on wave forms, the PMD-controlled item is the 2's complement and the AMD-controlled item is binary.



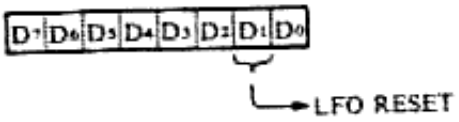
F = 1 . . PMD

F = 0 . . AMD

- TEST* (LFO RESET)

  The LFO output wave form is reset by entering "1" or "0" int the bits depicted in the diagram below from among the test signals when turning on the unit. The process will restart from the left edge of the previous wave form, providing synchronization once the various modulations are activated

  - NOTE: This is a TEST-use signal; entering level "1" data in a place other than the designated bit will cause the device to into the test mode.

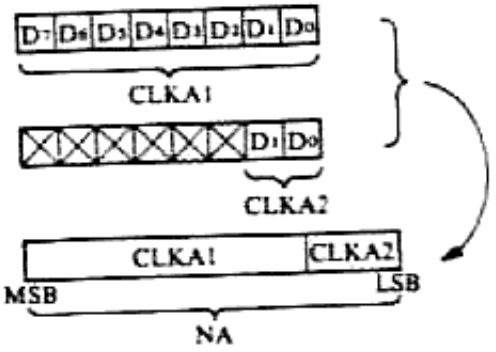


2.1.7 Timer

The Timer actually consists of two different timers: a pre-set 10-bit Timer A and a pre-set 8-bit Timer B. Both timers can be started and stopped. When there is an overflow, these timers function to insert a flag into the data bus. Also, for Timer A there is a key-on function that is activated when there is an overflow. At this point it is necessary stop the interrupt, and there is a control for this as well.

- CLKA1/CLKA2

  As indicated in the following diagram, these are composed of 2 words of 10 bits. With these, Timer A generates an overflow at the indicated period.

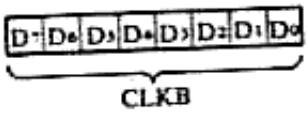


$$T_A\ (ms) = \frac{64*(1024-NA)}{\phi_M\ (KHz)}$$

□ $\phi_M = 3579.545KHz$ (YM2151 added clock frequency)

- CLKB

  Composed of 8 bits as indicated in the following diagram. With these, Timer B generates an overflow at the indicated period.

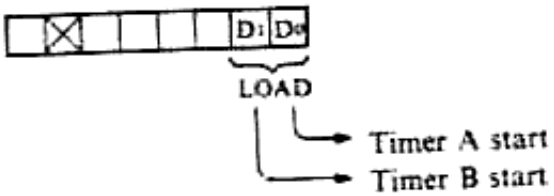


$$T_B\ (ms) = \frac{1024 \bullet (256\text{-}CLKB)}{\phi_M\ (KHz)}$$

□ $\phi M = 3579.545KHz$ (YM2151 added clock frequency)

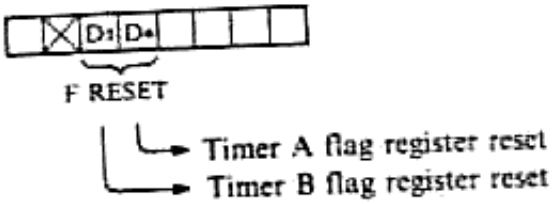
- LOAD

  The start/stop action of timers A and B is controlled with the 2 bits depicted in the following figure. Entering "1" starts the timers, while entering "0" stops them.



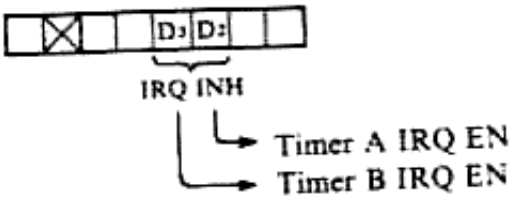
- F RESET

  These 2 bits reset the flag register contents indicating that the timers mentioned previously have generated an overflow ("1" resets).



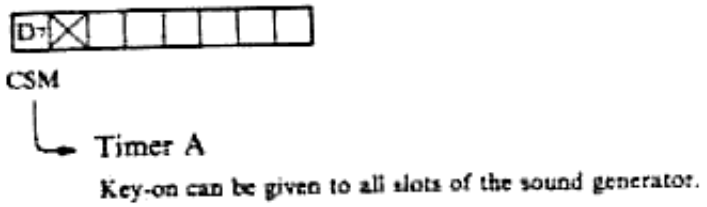
- IRQ EN

  These 2 bits enable you to inhibit the flag register indicating that the Timers mentioned previously have generated an overflow.



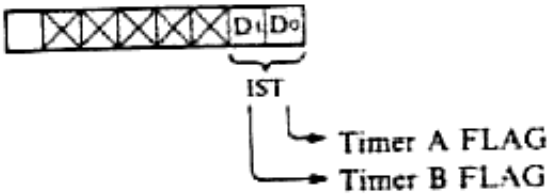
- CSM

  Entering "1" in this slot enables you to enter a key-on in all sound source slots when Timer A generates an overflow.



- IST: (READ MODE)

  The 2 bits to be discussed below indicate the status of the flag register. When the IRQ pin terminal reads "0", one of the 2 flag registers will indicate that the overflow from either Timer A or Timer B and that the level status reads "1".



2.1.8 ACC: Accumulator

This functional unit takes the L/R control signal from the register, inputs the musical signal data into either the L sequence or the R sequence, or into both the L and R sequences simultaneously, and accumulates it. The accumulated L/R sequence signals are then alternately output to the serial in mantissa 10- bit (including the sine bit) and index 3-bit offset binary format from the LSB. (Refer to Figure 2.17.)

- LR: LEFT CHANNEL ENABLE/RIGHT CHANNEL ENABLE

  This is the control signal for used to divide the 2-bit signal from the OP between the Left and Right sequences or input it t the simultaneous dual accumulator, as indicated in the following figure.

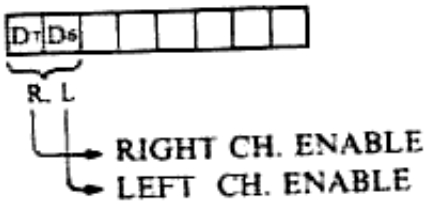


Fig. 2.1 Block Diagram

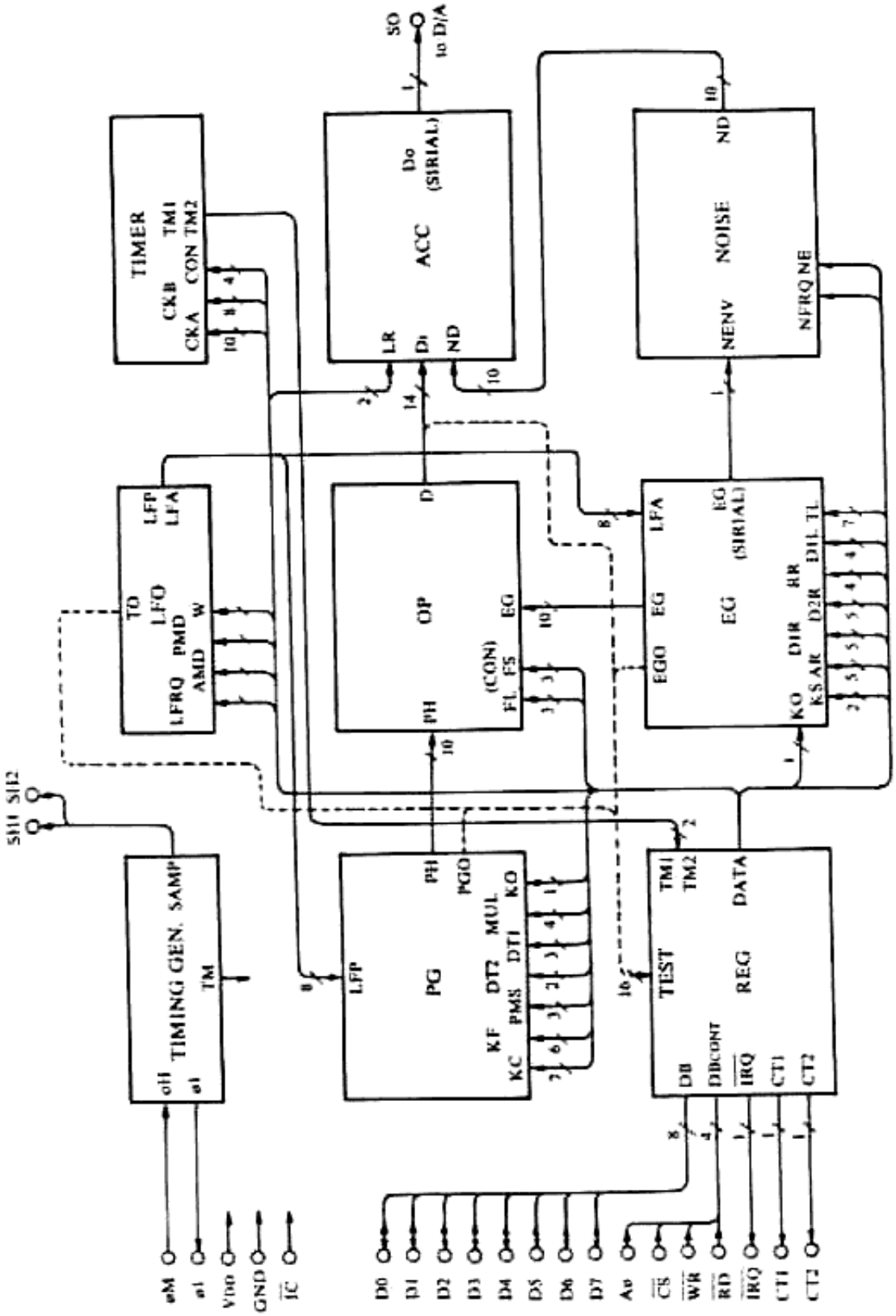


Fig. 2.2 Slot Designations

FUNCTION	M1	M2	C1	C2
	Modulator 1	Modulator 2	Carrier1	Carrier2
SLOT No.	1 2 3 4 5 6 7 8	9 10 11 12 13 14 15 16	17 18 19 20 21 22 23 24	25 26 27 28 29 30 31 32
CH No.	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8	1 2 3 4 5 6 7 8

When the NOISE control is set at ENABLE, this slot changes t become the noise slot.

Fig. 2.3 a)
Address Map (1); WRITE MODE

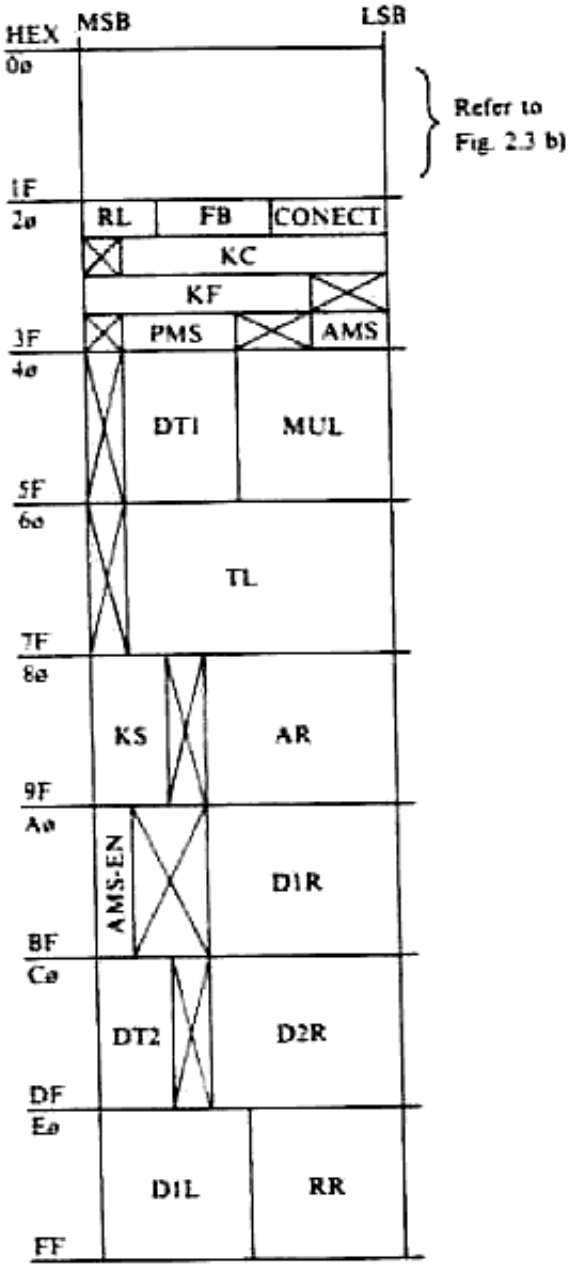


Fig. 2.3 b)
Address Map (2); WRITE MODE

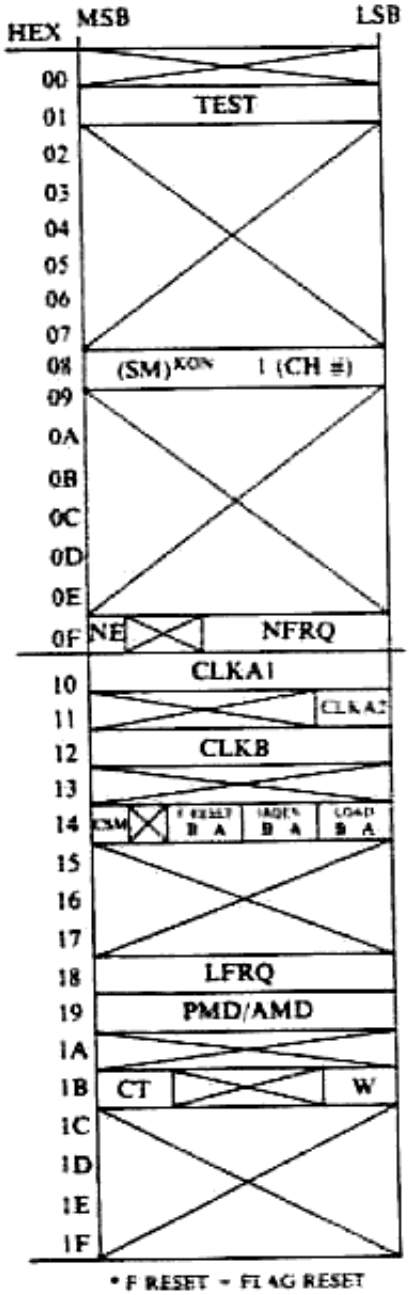


Fig. 2.3 c) Address Map (3); READ MODE

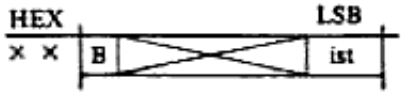


Fig. 2.4 KEY CODE, KEY FRACTION

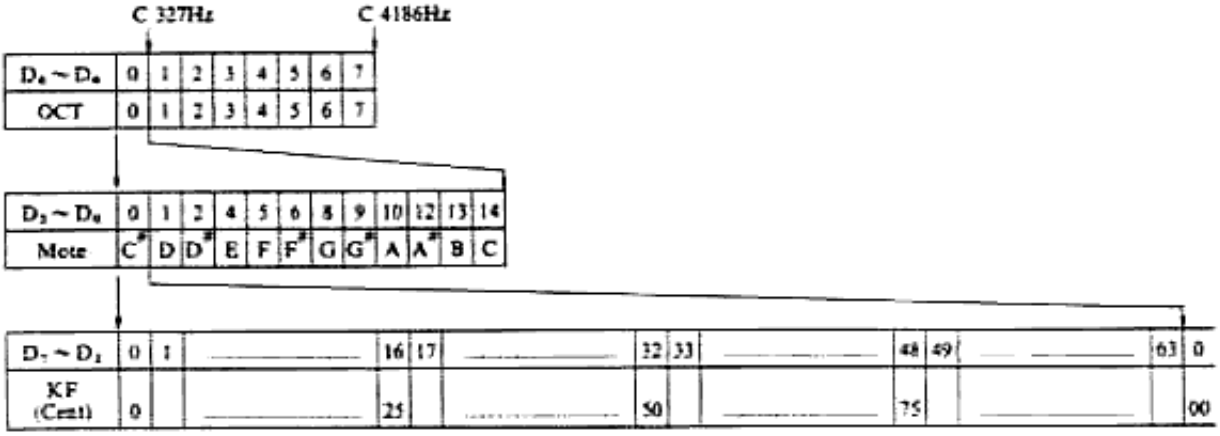


Fig. 2.5 PHASE MULTIPLY

MUL = ($D_3 \sim D_0$)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MULTIPLY	0.5	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Fig. 2.6 DETUNE(1) DT1 = (D_7-D_4), OCT = (D_6-D_4), NOTE = (D_3-D_2)

OCT	NOTE	DT1=0 D-CENT	DT1=1	DT1=2	DT1=3	DT1=0 D-FREQ (Hz)	DT1=1	DT1=2	DT1=3
0	0	0.000	0.000	5.025	10.036	0.000	0.000	0.053	0.107
0	1	0.000	0.000	4.228	8.445	0.000	0.000	0.053	0.107
0	2	0.000	0.000	3.559	7.110	0.000	0.000	0.053	0.107
0	3	0.000	0.000	2.993	5.980	0.000	0.000	0.053	0.107
1	0	0.000	2.515	5.025	5.025	0.000	0.053	0.107	0.107
1	1	0.000	2.115	4.228	6.338	0.000	0.053	0.107	0.160
1	2	0.000	1.778	3.555	5.330	0.000	0.053	0.107	0.160
1	3	0.000	1.496	2.990	4.483	0.000	0.053	0.107	0.160
2	0	0.000	1.258	2.515	5.025	0.000	0.053	0.107	0.213
2	1	0.000	1.057	3.170	4.225	0.000	0.053	0.160	0.213
2	2	0.000	0.889	2.667	3.555	0.000	0.053	0.160	0.213
2	3	0.000	0.748	2.242	3.735	0.000	0.053	0.160	0.267
3	0	0.000	1.258	2.515	3.143	0.000	0.107	0.213	0.267
3	1	0.000	1.057	2.114	3.170	0.000	0.107	0.213	0.320
3	2	0.000	0.889	1.778	2.667	0.000	0.107	0.213	0.320
3	3	0.000	0.748	1.869	2.615	0.000	0.107	0.267	0.373
4	0	0.000	0.629	1.572	2.515	0.000	0.107	0.267	0.427
4	1	0.000	0.793	1.586	2.114	0.000	0.160	0.320	0.427
4	2	0.000	0.667	1.334	2.001	0.000	0.160	0.320	0.480
4	3	0.000	0.561	1.308	1.869	0.000	0.160	0.373	0.533
5	0	0.000	0.629	1.258	1.729	0.000	0.213	0.427	0.587
5	1	0.000	0.529	1.057	1.586	0.000	0.213	0.427	0.640
5	2	0.000	0.445	1.001	1.445	0.000	0.213	0.480	0.693
5	3	0.000	0.467	0.935	1.308	0.000	0.267	0.533	0.747
6	0	0.000	0.393	0.865	1.258	0.000	0.267	0.587	0.853
6	1	0.000	0.397	0.793	1.123	0.000	0.320	0.640	0.907
6	2	0.000	0.334	0.723	1.056	0.000	0.320	0.693	1.013
6	3	0.000	0.327	0.654	0.935	0.000	0.373	0.747	1.067
7	0	0.000	0.315	0.629	0.865	0.000	0.427	0.853	1.173
7	1	0.000	0.264	0.562	0.865	0.000	0.427	0.907	1.173
7	2	0.000	0.250	0.528	0.865	0.000	0.480	1.013	1.173
7	3	0.000	0.234	0.467	0.865	0.000	0.533	1.067	1.173

Fig. 2.7 DETUNE(2)

DT2 = (D--D₄)		0	1	2	3
DETUNE	(cent)	0	+600	+781	+950
	(×)	1	+1.41	+1.57	+1.73

Fig. 2.8 PHASE MODULATION SENSITIVITY

PMS = (D₆-D₄)	0	1	2	3	4	5	6	7
MOD MAX (cent)	0	±5	±10	±20	±50	±100	±400	±700

Fig. 2.9 CONNECTION = (FS)

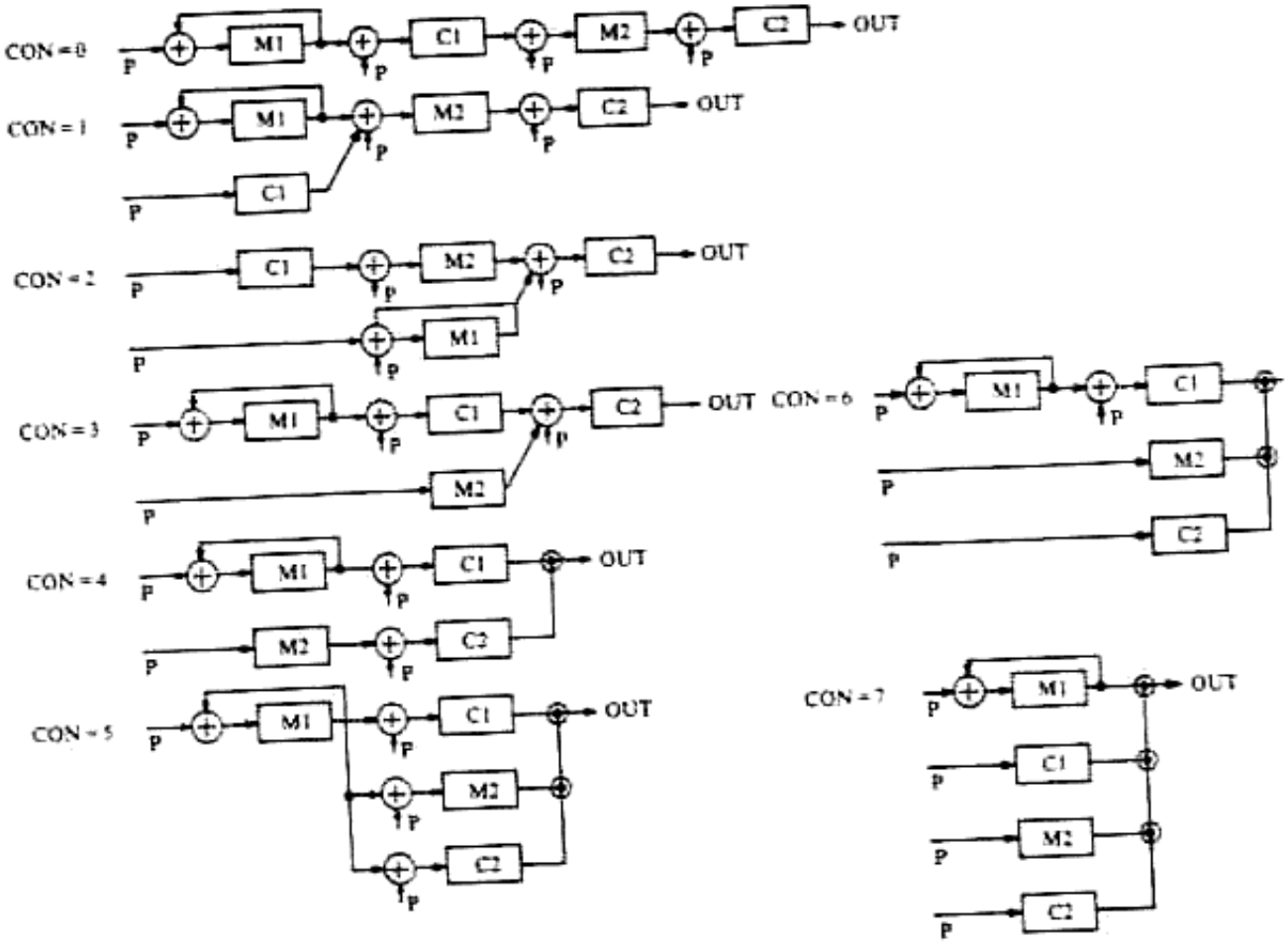


Fig. 2.10 SELF FEED BACK LEVEL

FL = (D₃-D₁)	0	1	2	3	4	5	6	7
LEVLE	OFF	π/16	π/8	π/4	π/2	π	2π	4π

Fig. 2.11 ATTACK, DECAY TIME

- In Figure 2.12, the 6 bits of the RATE after they have undergone key scaling are divided in two parts and are thus expressed as the first 4 bits and the last 2 bits.

- The "(10%~90%)" and "(90%~10%)" tables express the amount of time it takes for the level to reach 90% from 10% and from 90% to 10%.

- The "(96 dB~0 dB)" and "(0 dB~96 dB)" tables express the amount of time it takes for the level to reach 100% from 0% and from 100% to 0%.

- NOTE: These tables assume ϕ_H = 3.6 MHz.

*** EG ATTACK TIME ***		*** EG DECAY TIME ***		*** EG ATTACK TIME ***		*** EG DECAY TIME ***	
RATE	mSEC (10%-90%)	RATE	mSEC (90%-10%)	RATE	mSEC (96dB-0dB)	RATE	mSEC (0dB-96dB)
15 3	0.00	15 3	1.36	15 3	0.00	15 3	6.73
15 2	0.27	15 2	1.36	15 2	0.53	15 2	6.73
15 1	0.27	15 1	1.36	15 1	0.53	15 1	6.73
15 0	0.27	15 0	1.36	15 0	0.53	15 0	6.73
14 3	0.34	14 3	1.55	14 3	0.66	14 3	7.69
14 2	0.39	14 2	1.81	14 2	0.75	14 2	8.97
14 1	0.47	14 1	2.18	14 1	0.90	14 1	10.76
14 0	0.39	14 0	2.72	14 0	1.12	14 0	13.45
13 3	0.62	13 3	3.11	13 3	1.22	13 3	15.38
13 2	0.73	13 2	3.63	13 2	1.42	13 2	17.94
13 1	0.87	13 1	4.35	13 1	1.71	13 1	21.53
13 0	1.09	13 0	5.44	13 0	2.13	13 0	26.91
12 3	1.25	12 3	6.22	12 3	2.22	12 3	30.75
12 2	1.46	12 2	7.25	12 2	2.60	12 2	35.88
12 1	1.75	12 1	8.70	12 1	3.11	12 1	43.05
12 0	2.19	12 0	10.88	12 0	3.89	12 0	53.81
11 3	2.50	11 3	12.43	11 3	4.45	11 3	61.50
11 2	2.92	11 2	14.51	11 2	5.19	11 2	71.75
11 1	3.50	11 1	17.41	11 1	6.23	11 1	86.10
11 0	4.37	11 0	21.76	11 0	7.79	11 0	107.63
10 3	5.00	10 3	24.87	10 3	8.90	10 3	123.00
10 2	5.83	10 2	29.01	10 2	10.38	10 2	143.50
10 1	7.00	10 1	34.82	10 1	12.46	10 1	172.20
10 0	8.75	10 0	43.52	10 0	15.57	10 0	215.25
9 3	10.00	9 3	49.74	9 3	17.80	9 3	246.00
9 2	11.66	9 2	58.03	9 2	20.76	9 2	287.00
9 1	13.99	9 1	69.63	9 1	24.92	9 1	344.41
9 0	17.49	9 0	87.04	9 0	31.15	9 0	430.51
8 3	19.99	8 3	99.47	8 3	35.60	8 3	492.01
8 2	23.32	8 2	116.05	8 2	41.53	8 2	574.01
8 1	27.99	8 1	139.26	8 1	49.83	8 1	688.81
8 0	34.99	8 0	174.08	8 0	62.29	8 0	861.01
7 3	39.98	7 3	198.95	7 3	71.19	7 3	984.02
7 2	46.65	7 2	232.11	7 2	83.06	7 2	1148.02
7 1	55.98	7 1	278.53	7 1	99.67	7 1	1377.62
7 0	69.97	7 0	348.16	7 0	124.59	7 0	1722.03
6 3	79.97	6 3	397.90	6 3	142.38	6 3	1968.03
6 2	93.30	6 2	464.21	6 2	166.12	6 2	2296.04
6 1	111.96	6 1	557.06	6 1	199.34	6 1	2755.24
6 0	139.93	6 0	696.32	6 0	249.17	6 0	3444.05
5 3	159.94	5 3	795.79	5 3	284.77	5 2	3926.06
5 2	186.60	5 2	928.43	5 2	332.23	5 2	4592.07
5 1	223.91	5 1	1114.11	5 1	398.68	5 1	5510.49
5 0	279.89	5 0	1392.64	5 0	498.33	5 0	6898.11
4 3	319.88	4 3	1591.59	4 3	569.54	4 3	7872.12
4 2	373.19	4 2	1856.85	4 2	664.46	4 2	9184.14
4 1	447.83	4 1	2228.22	4 1	797.35	4 1	11029.97
4 0	559.79	4 0	2785.28	4 0	996.69	4 0	13776.21
3 3	639.76	3 3	3183.18	3 3	1139.08	3 3	15744.24
3 2	746.38	3 2	3713.71	3 2	1328.92	3 2	18368.28
3 1	895.66	3 1	4456.45	3 1	1594.71	3 1	22041.94
3 0	1119.57	3 0	5570.56	3 0	1993.39	3 0	27552.43
2 3	1279.51	2 3	6366.35	2 3	2278.16	2 3	31488.49
2 2	1492.76	2 2	7427.41	2 2	2657.83	2 2	36736.57
2 1	1791.32	2 1	8912.70	2 1	3189.43	2 1	44083.88
2 0	2239.13	2 0	11141.12	2 0	3986.77	2 0	55104.83
1 3	2559.02	1 3	12732.71	1 3	4556.31	1 3	62976.98
1 2	2985.53	1 2	14854.83	1 2	5315.70	1 2	73473.14
1 1	3582.63	1 1	17825.79	1 1	6378.84	1 1	88167.77
1 0	4478.29	1 0	22282.24	1 0	7973.55	1 0	110209.71
0 3	INFINITY	0 3	INFINITY	0 3	INFINITY	0 3	INFINITY
0 2	INFINITY	0 2	INFINITY	0 2	INFINITY	0 2	INFINITY
0 1	INFINITY	0 1	INFINITY	0 1	INFINITY	0 1	INFINITY
0 0	INFINITY	0 0	INFINITY	0 0	INFINITY	0 0	INFINITY

Fig. 2.12 KEY SCALING

(•) RATEs that have undergone key scaling have doubled the input rate (R) and added the values listed in the table below (RKS).

(••) AR, D1R, and D2R use the values entered in the register for input rate (R). However, for RR a calculation of double the values entered in the register plus 1 has been used for the input rate (R).

$$RATE = 2 \bullet R + RKS$$

When calculation results yield a value greater than 63, assume all RATEs = 63.

- R: Input rates
- RKS: The values listed in the following table, found by using the KEY CODE and KS.
- However, the KEY CODE used here refers to the KC' of the last 2 detached bits of a note, as indicated in the following diagram.

KC'	KS 0	KS 1	KS 2	KS 3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	2
3	0	0	1	3
4	0	1	2	4
5	0	1	2	5
6	0	1	3	6
7	0	1	3	7
8	1	2	4	8
9	1	2	4	9
10	1	2	5	10
11	1	2	5	11
12	1	3	6	12
13	1	3	6	13
14	1	3	7	14
15	1	3	7	15
16	2	4	8	16
17	2	4	8	17
18	2	4	9	18
19	2	4	9	19
20	2	5	10	20
21	2	5	10	21
22	2	5	11	22
23	2	5	11	23
24	3	6	12	24
25	3	6	12	25
26	3	6	13	26
27	3	6	13	27
28	3	7	14	28
29	3	7	14	29
30	3	7	15	30
31	3	7	15	31

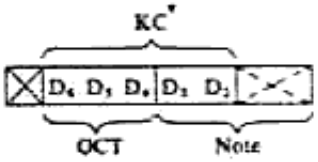
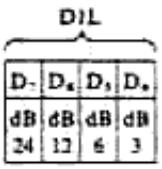


Figure 2.13 Bits and weighting of the First DECAY LEVEL



• The decay level value of 48 dB will be added if D7 through D4 are ALL "1" = 45 dB.

Figure 2.14 Bits and weighting of TOTAL LEVEL

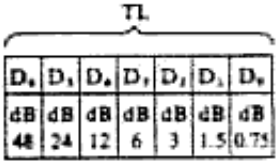


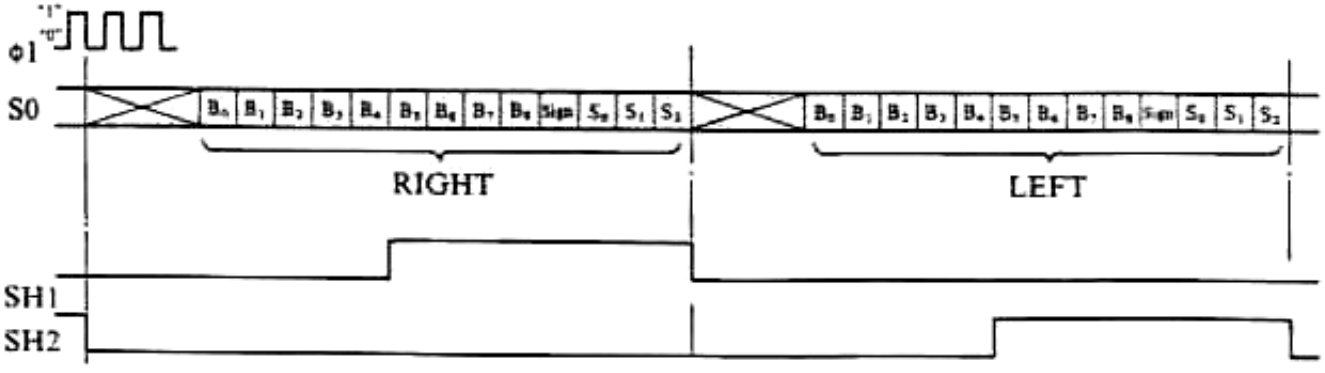
Figure 2.15 AMPLITUDE MODULATION SENSITIVITY

AMS	AM MOD (MAX)
0	0
1	23.90625 dB
2	47.8125 dB
3	95.625 dB

Fig. 2.16 LOW FREQ. OSC

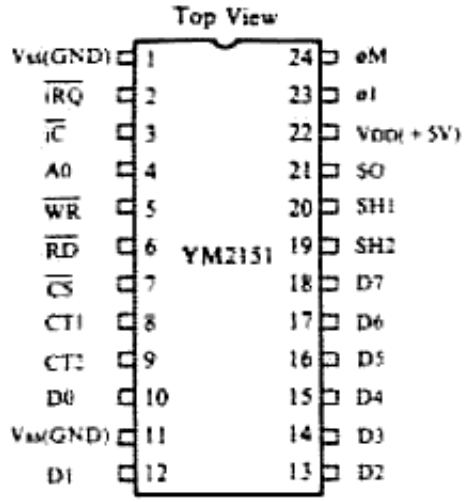
DATA (HEX)	FREQ. (Hz)	DATA (HEX)	FREQ. (Hz)	DATA (HEX)	FREQ. (Hz)	DATA (HEX)	FREQ. (Hz)
FF	32.9127	BF	3.3070	7F	0.2067	3F	0.0129
FE	31.2058	BE	3.2004	7E	0.2000	3E	0.0125
FD	49.4989	BD	3.0937	7D	0.1934	3D	0.0121
FC	47.7921	BC	2.9870	7C	0.1867	3C	0.0117
FB	46.0852	BB	2.8803	7B	0.1800	3B	0.0113
FA	44.3784	BA	2.7736	7A	0.1734	3A	0.0108
F9	42.6715	B9	2.6670	79	0.1667	39	0.0104
F8	40.9646	B8	2.5603	78	0.1600	38	0.0100
F7	39.2578	B7	2.4536	77	0.1534	37	0.0096
F6	37.5509	B6	2.3469	76	0.1467	36	0.0092
F5	35.8441	B5	2.2403	75	0.1400	35	0.0088
F4	34.1372	B4	2.1336	74	0.1333	34	0.0083
F3	32.4303	B3	2.0269	73	0.1267	33	0.0079
F2	30.7235	B2	1.9202	72	0.1200	32	0.0075
F1	29.0166	B1	1.8135	71	0.1133	31	0.0071
F0	27.3098	B0	1.7069	70	0.1067	30	0.0067
EF	26.4563	AF	1.6535	6F	0.1033	2F	0.0065
EE	25.6029	AE	1.6002	6E	0.1000	2E	0.0063
ED	24.7495	AD	1.5468	6D	0.0967	2D	0.0060
EC	23.8960	AC	1.4935	6C	0.0933	2C	0.0058
EB	23.0426	AB	1.4402	6B	0.0900	2B	0.0056
EA	22.1892	AA	1.3868	6A	0.0867	2A	0.0054
E9	21.3358	A9	1.3335	69	0.0833	29	0.0052
E8	20.4823	A8	1.2801	68	0.0800	28	0.0050
E7	19.6289	A7	1.2268	67	0.0767	27	0.0048
E6	18.7755	A6	1.1735	66	0.0733	26	0.0046
E5	17.9221	A5	1.1201	65	0.0700	25	0.0044
E4	17.0686	A4	1.0668	64	0.0667	24	0.0042
E3	16.2152	A3	1.0134	63	0.0633	23	0.0040
E2	15.3617	A2	0.9601	62	0.0600	22	0.0038
E1	14.5083	A1	0.9068	61	0.0567	21	0.0035
E0	13.6549	A0	0.8534	60	0.0533	20	0.0033
DF	13.2282	9F	0.8268	5F	0.0517	1F	0.0032
DE	12.8015	9E	0.8001	5E	0.0500	1E	0.0031
DD	12.3747	9D	0.7734	5D	0.0483	1D	0.0030
DC	11.9480	9C	0.7468	5C	0.0467	1C	0.0029
DB	11.5213	9B	0.7201	5B	0.0450	1B	0.0028
DA	11.0946	9A	0.6934	5A	0.0433	1A	0.0027
D9	10.6679	99	0.6667	59	0.0417	19	0.0026
D8	10.2412	98	0.6401	58	0.0400	18	0.0025
D7	9.8144	97	0.6134	57	0.0383	17	0.0024
D6	9.3877	96	0.5867	56	0.0367	16	0.0023
D5	8.9610	95	0.5601	55	0.0350	15	0.0022
D4	8.5343	94	0.5334	54	0.0333	14	0.0021
D3	8.1076	93	0.5067	53	0.0317	13	0.0020
D2	7.6809	92	0.4801	52	0.0300	12	0.0019
D1	7.2542	91	0.4534	51	0.0283	11	0.0018
D0	6.8274	90	0.4267	50	0.0267	10	0.0017
CF	6.6141	8F	0.4134	4F	0.0258	0F	0.0016
CE	6.4007	8E	0.4000	4E	0.0250	0E	0.0016
CD	6.1874	8D	0.3867	4D	0.0242	0D	0.0015
CC	5.9740	8C	0.3734	4C	0.0233	0C	0.0015
CB	5.7607	8B	0.3600	4B	0.0225	0B	0.0014
CA	5.5473	8A	0.3467	4A	0.0217	0A	0.0014
C9	5.3339	89	0.3334	49	0.0208	09	0.0013
C8	5.1206	88	0.3200	48	0.0200	08	0.0013
C7	4.9072	87	0.3067	47	0.0192	07	0.0012
C6	4.6939	86	0.2934	46	0.0183	06	0.0011
C5	4.4805	85	0.2800	45	0.0175	05	0.0011
C4	4.2672	84	0.2667	44	0.0167	04	0.0010
C3	4.0538	83	0.2534	43	0.0158	03	0.0010
C2	3.8404	82	0.2400	42	0.0150	02	0.0009
C1	3.6271	81	0.2267	41	0.0142	01	0.0009
C0	3.4137	80	0.2134	40	0.0133	00	0.0008

Fig. 2.17 SO, φ1, SH1, SH2: TIMING



2.2 Pin Wiring

The YM2151 uses a 24-lead dual in-line package. The terminal signals are indicated in the following diagram.



2.2.1 Pin Functions

- $D_0 \sim D_7$: Address/Data Bus (input/output high impedance)
  A multiplex bus that can be used for both address and data; inputs an 8-bit parallel signal between an external device and the internal register.

- A0 : Address/Data Select (Input)
  When A0 = "0", the $D_0 \sim D_7$ signal is processes as an address signal; when A0 = "1", the $D_0 \sim D_7$ signal is processed as data.

- $\overline{WR}$: Write (Input)
  When there is a write signal, the signals in the bus can be entered.

- $\overline{RD}$: Read (Input)
  When there is a read signal, the internal signals can be read out via the bus.

- $\overline{CS}$: Chip Select (Input)
  When there is a chip select signal, the A0, $\overline{WR}$, and $\overline{RD}$ signals become operative and the $D_0 \sim D_7$ bus data can be entered in the internal register or internal data can be read out on the $D_0 \sim D_7$ bus.

- $\overline{IC}$: Initial clear (Input)
  Internal registers and circuits are initialized when this terminal reads "0".

- $\overline{IRQ}$: Interrupt request (Output: Open drain)
  If either of the 2 types of timer counters begins a carry out, this signal will read out a "0" level and request an interrupt from the CPU. Then, with the CPU's readout of the data, the unit will determine from which timer the interrupt request has been made and will process the interrupt.

- CT1, CT2: Control 1, Control 2 (Output)
  This is the terminal that is used to control an external device and should read "0" level when at initial condition.

- SO: Serial Output (Output)
  Takes the tone signal divided between the 2 left and right channels, outputs it as serial data, and sends it to the YM3012 D/A converter specially developed for use with the YM2151.

- SH1, SH2: Sample and hold
  Used to pick up the serial data supplied to the YM3012 D/A converter, and for sampling hold after analog conversion.

- ϕM: System clock (Input)
  Inputs the clock ϕM that drives the YM2151, which is internally broken down to and used at 1/2 the frequency. The ϕM is the reference for the tone signal.

- ϕ1: Clock for D/A (Output)
  This clock drives the D/A and operates at the same frequency as the clock inside the YM2151. Also, when the ϕ1 level shifts from "1" to "0", the IRQ, CT1, CT2, TO, SH1, SH2, and SO signals all change

- V_{DD}: Power Supply (Input)
  Normally supplies at +5V.

- Vss: Grand (Input)
  Conects the system grand.

3. DEVICE SPECIFICATION

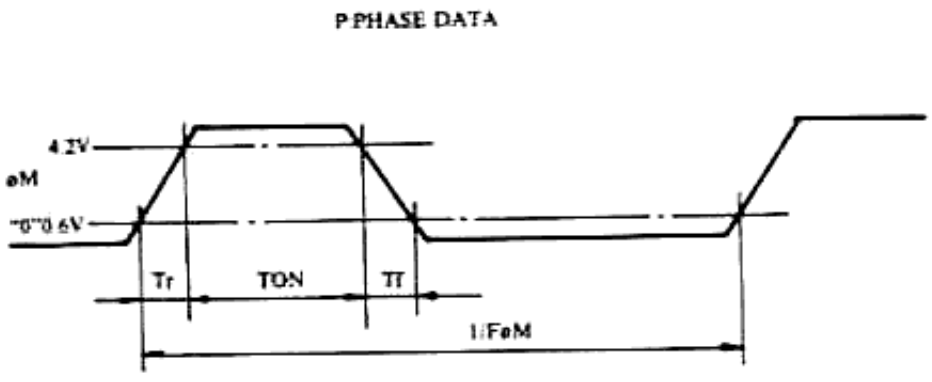
3.1 Maximum Ratings

Voltage Range	−0.3V ~ + 7 V
Operating temperature	0 °C ~ + 70°C
Storage temperature	− 50 °C ~ +125°C

3.2 Electrical Characteristics

		[MIN]	[TYP]	[MAX]	
1) operating supply voltage (Vss to V_{DD})		4.75		5.25	V
2) clock [ϕM]					
Voltage level	"0"	−0.3		0.8	V
Voltage level	"1"	2.0		V_{DD}	V
Rise time (Fig.3-1)	Tr			50	ns
Fall time (Fig.3-1)	Tf			50	ns
ON time (Fig.3-1)	Ton	100			ns
Frequency	FϕM	3.0	3.58	4.0	MHz
Input capacitance	CϕM			10	pF

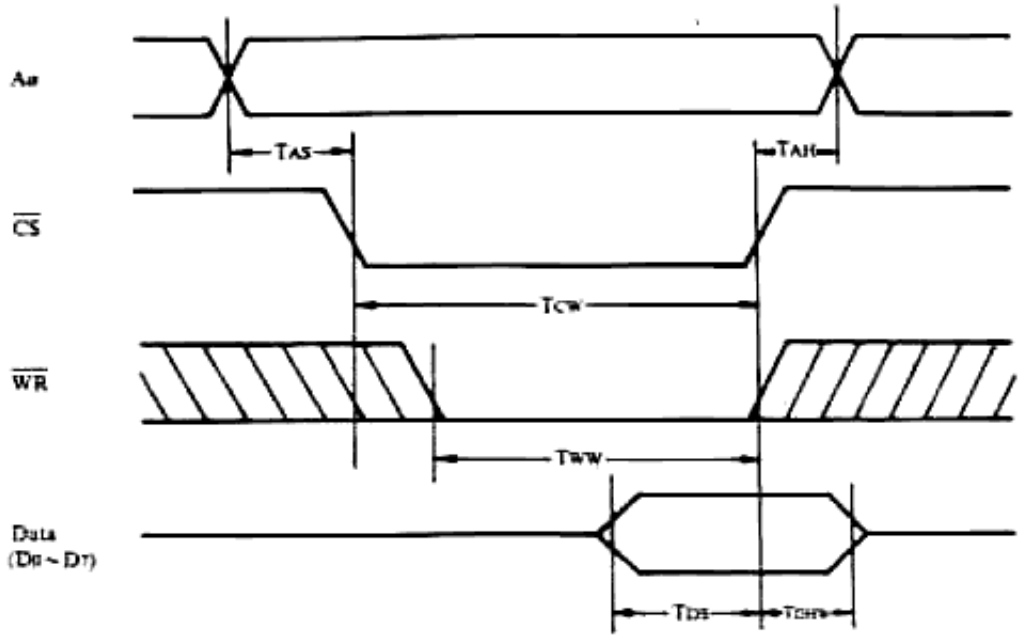
Fig. 3-1



		[MIN]	[TYP]	[MAX]	
3) ALL INPUT					
Voltage level "0"		−0.3		0.8	V
Voltage level "1"		2.0		V_{DD}	V
4) ALL OUTPUT					
Voltage level "0"		−0.3		0.4	V
Voltage level "1"		2.4		V_{DD}	V
5) [A0, $\overline{WR}$, $\overline{RD}$, φM]					
Input Leak Current (Fig.3-5) I_L (at 25°C Vi = 0-V_{DD})		−10		10	μA
6) [$\overline{IC}$, $\overline{CS}$]					
Input Current (Fig.3-6) Iiφ (at V_{DD} = 5V)		10		60	μA
7) [$\overline{IRQ}$*, CT1, CT2, D0-D7, SH1, SH2, SO, φ1]					
Load Current (Fig.3-7) I_D (at V_{LO} = 0.4V)				2.1	mA
* OPEN DRAIN					
8) WRITE/READ TIMING (Fig.3-2a, Fig.3-2b)					
Address Set-up Time	(T_{AS})	10			ns
Address Hold Time	(T_{AH})	10			ns
$\overline{CS}$ WRITE WIDTH	(T_{CW})	100			ns
$\overline{WR}$ WRITE WIDTH	(T_{WN})	100			ns
WRITE DATA Set-up Time	(T_{DS})	50			ns
WRITE DATA Hold Time	(T_{DHW})	10			ns
READ DATA Access Time	(T_{ACC})			180	ns
READ DATA Hold Time	(T_{DHR})	10			ns

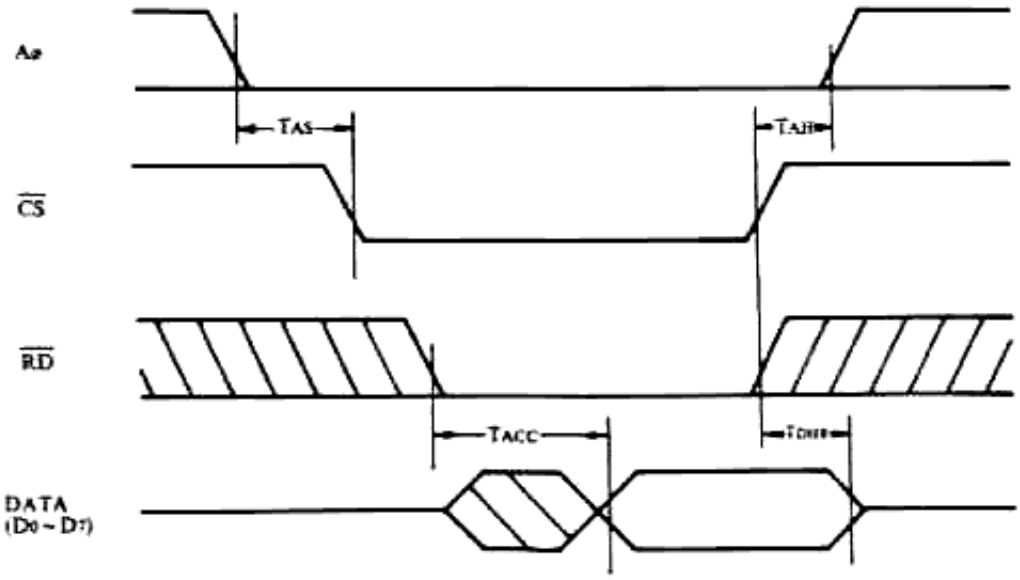
	[MIN]	[TYP]	[MAX]	
9) [φ1]				
Rise time (Fig.3-3) T_{r1}			180	ns
Fall time (Fig.3-3) T_{f1}			120	ns
Load capacitance CL (Fig.3-7)			100	pF
10) [$\overline{IRQ}$, CT1, CT2, SO, SH1, SH2]				
Rise time (Fig.3-3) Tr			250	ns
Fall time (Fig.3-3) Tf			250	ns
Load capacitance CL (Fig.3-7)			100	pF
11) POWER Supply current I_{DD}			120	mA
12) POWER Dispation P_D (at V_{DD} = 5.25V)			630	mW

Fig. 3-2a WRITE TIMING



NOTE: TDS and TDHN use as a reference either $\overline{CS}$ or $\overline{WR}$, whichever has attained High Level.

Fig. 3-2b READ TIMING



NOTE: TACC uses as a reference either $\overline{CS}$ or $\overline{RD}$, whichever is the last to attain Low Level.
TDHR uses as a reference either $\overline{CS}$ or $\overline{RD}$, whichever has attained High Level.

Fig. 3-3

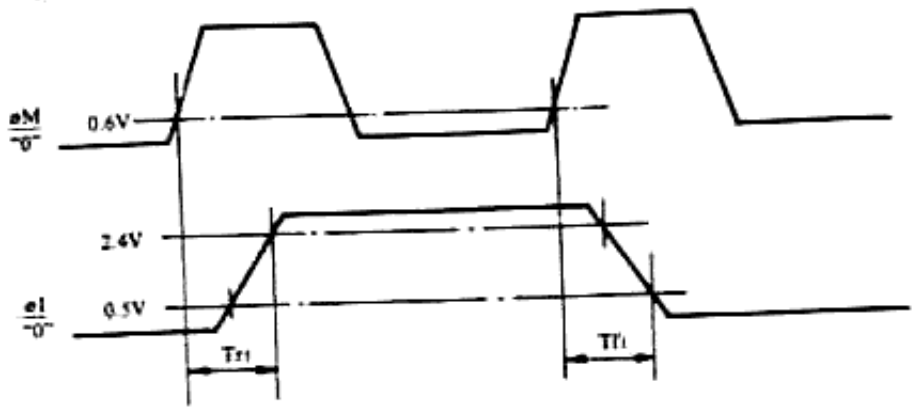


Fig. 3-4

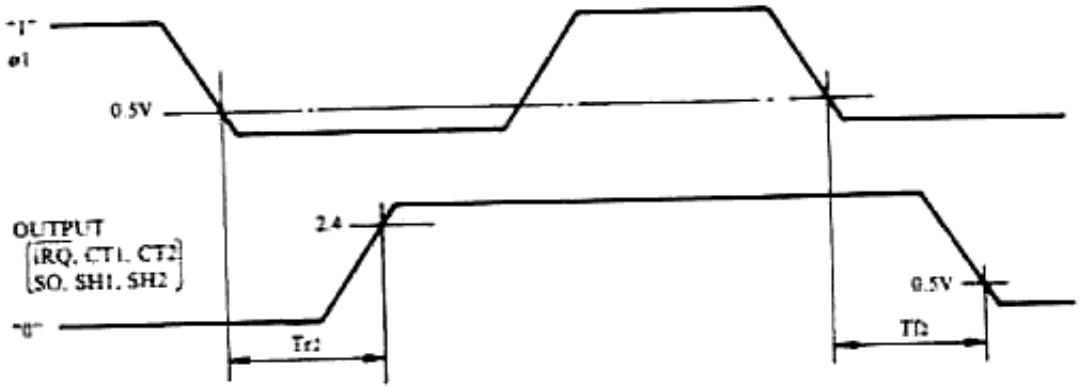


Fig. 3-5

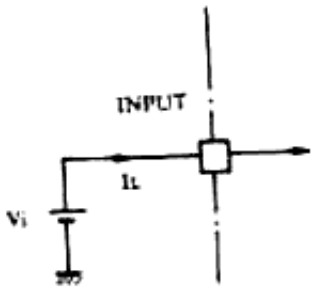


Fig. 3-6

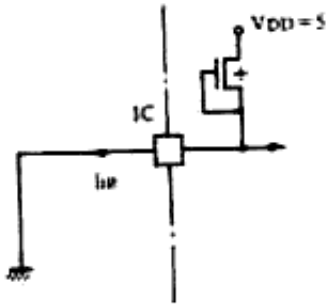


Fig. 3-7

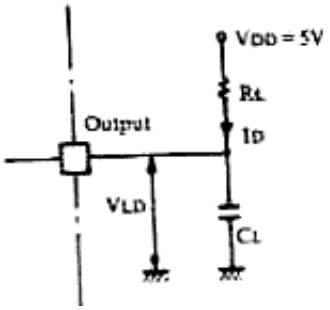


Fig. 4.1 SYSTEM BLOCK DIAGRAM

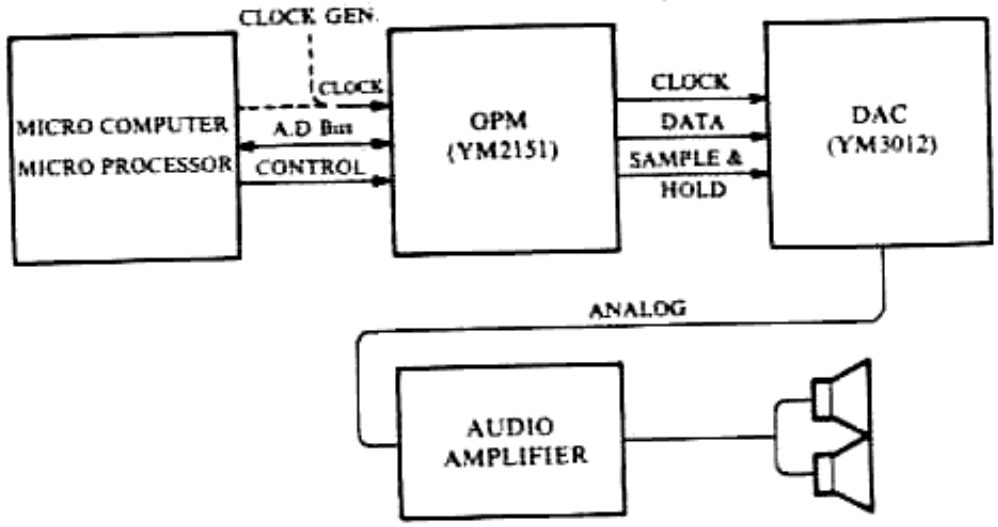
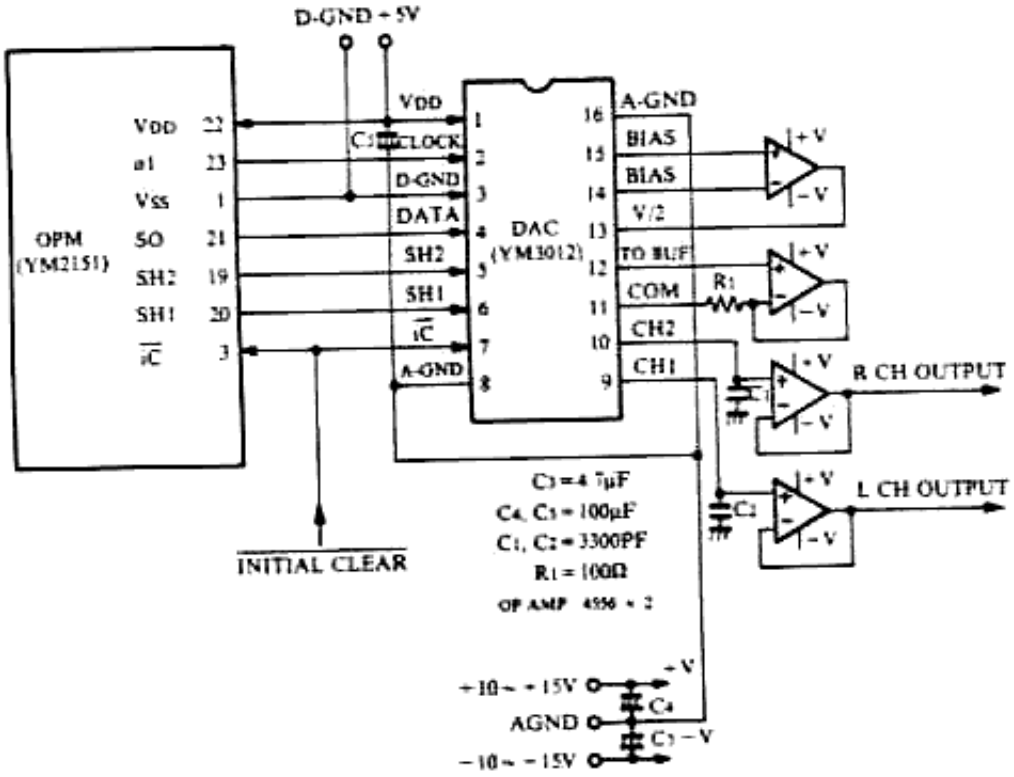


Fig. 4.2 DAC INTERFACE



4. INTERFACING

Figure 4.1 is a block diagram of the basic configuration of the unit, including the microprocessor or microcomputer, DA converter, and speakers, in addition to the YM2151. As it is possible that you may alter the data if you operate this device without synchronizing it with the microprocessor or microcomputer, you can drive the unit by using a separate clock generator to achieve the required sound levels.

With the YM2151 and the DAC configurated as shown in Figure 4.2, you can have both left and right, 2-channel output.